



Step Up and Step Down Converter Based On Three State Switching Cell for High Power Applications

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ABSTRACT: This paper presents a step up and step down dc to dc converter based on the three state switching cell. It can be used for high power applications. The circuit consists of two switches two diodes and two coupled inductors. This topology has 3 switching stages, thus the name given as three state switching cell. In this circuit only part of load power is transferred by the switches so switching stress is less and high power output up to 1.5 KW can be attained. Advantages of this topology are less size and volume of components, wide area of continuous conduction mode. Step up and step down converter have overlapping and non-overlapping modes. When duty ratio is less than 0.5, we can achieve non-overlapping and continuous conduction mode. Input voltage is taken as 200V, in buck converter 60V output and in boost converter 282V output is obtained at duty ratio 0.3. Simulations are done in SIMULINK/MATLAB.

KEYWORDS: Buck Converter, Boost Converter, DC-DC Converters, Three State Switching Cell (3SSC)

I. INTRODUCTION

Pulse-width modulated (PWM) converters are currently used in the majority of DC-DC conversion applications. Widespread applications of DC-DC converters include UPS, variety of electronic systems, energy systems for telecommunications, systems for utilization of solar energy, DC motor drivers and energy systems for satellites. Also DC-DC converters are often found as basic building blocks for other types of power converters. This paper introduces a new family of PWM DC-DC non-isolated converters [1]. The new converters are generated using three-state commutation cells. Comprising two active switches, two diodes and coupled inductors. The main advantages over the classical converters are low conduction and commutation losses, and low input and output current ripple. Due to these features, the new converters are suitable for high voltage and high current applications. Earlier days, conventional dc-dc converters are used single switch and hard switching technique [2]. It has low power density and large switching losses.

To avoid above limitation, we use soft switching, so it reduces overlap between voltage and current [6]. And also we can use snubber circuit for reducing switching losses. This circuit integrates the advantage of reduced voltage across the switches using three level commutation cell, and decreased switching losses obtained from a soft switching technique. By using interleaving technique in high current applications, output ripples can be reduced [3]. This paper presents the method to obtain the three-state switching cells. The obtained cells are subsequently used to synthesize a new family of DC-DC three-state switching converters. In the last few years, many converters based on the three-state switching cell (3SSC) have been proposed. The cell can be obtained by the association of two 2-state PWM cells (2SSC) interconnected to a center tap autotransformer, from which novel converters can be derived. General advantages of 3SSC circuits over conventional topologies are, the inductor is designed for twice the switching frequency, with consequent reduction of size and the current through the switches is half of the input current. In the 3SSC circuits, part of the input power is delivered to the load by the transformer instead of the main switches, thus reducing conduction and commutation losses and lower cost switches can be used. Here we describe non-overlapping mode and continuous conduction period. When duty ratio is less than 0.5, non-overlapping mode can be attained.



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Evolution of 3SSC step up and step down converters can be described as, in earlier days classical dc-dc converters are used like buck, boost, buck –boost, buck etc. After these 2SSC circuits are invented, it has high power density and reduced size of reactive elements but switching losses are large so we use soft switching techniques. Using zero voltage converter (ZVS) or zero current switching (ZCS) switching losses are eliminated but conduction losses are present. To avoid conduction losses, we can use multilevel converters.

II. EVOLUTION OF 3SSC STEP UP AND STEP DOWN CONVERTER

3SSC converters are actually evolved from conventional push pull converters[4]. In order to make 3SSC buck and boost circuits, we can replace high frequency transformer into coupled inductors. For this we can assume the turns ratio of central tap autotransformer is unity and ideal. Also connect the negative pole of the output voltage stage to the input negative pole. Thus we can achieve a converter with less switching losses. Characteristics of the 3SSC converters are[1]: Reduced size, and volume of magnetics, which are redesigned for twice the switching frequency analogously to the interleaved buck converter. The current stress through each main switch is equal to half of the total output current, allowing the use of semiconductors with lower current ratings. Losses are distributed among the semiconductors, leading to better heat distribution and consequently more efficient use of the heat sinks. Part of the input power, i.e., 50%, is directly transferred to the load through the diodes and the coupled inductors (autotransformers), and not through the main switches. As a consequence, conduction and switching losses are reduced. This is the main difference between the functionality of this approach and that of the interleaved buck topology. The use of the 3SSC allows the parallel connection of switches and, therefore, inexpensive power devices and drives can be used. Energy is transferred from the source to the load during most part of the switching period, which is a distinct characteristic of the proposed converter, since in other buck type converters, it only occurs during half of the switching period. As a consequence, reduction of current peaks and also conduction losses are expected. The drive circuit of the main switches becomes less complex because they are connected to the same reference node, what does not occur in the interleaved buck converter.

Several assumptions have to be considered for the analysis of new 3SSC converters

- 1) Converters operate in steady state.
- 2) Switching frequency is constant and PWM is employed to drive the switches.
- 3) The gating signals of the switches are 180° displaced.
- 4) The turns ratio of the autotransformer is unity.
- 5) The magnetizing current is much lower than the load current.
- 6) All semiconductor and passive elements are ideal.

III. 3SSC BUCK CONVERTER AND BOOST CONVERTERS

3SSC buck and boost circuits consist of two diodes, two switches and two coupled inductors. Output voltage source consists of a snubber circuit. So circuit cost is increased and reliability is affected by using active snubbers so we use a passive lossless snubber. It effectively restricts switching losses and electromagnetic interference (EMI) noise using no active components and no power dissipative components[1]. 3SSC converters are evolved from conventional push pull dc – dc converter. Push pull converter consists of two diodes, two switches but secondary side consists of a high frequency transformer, here dc-ac-dc conversion occurred. By assuming unity turns ratio for the central tap autotransformer. So we can replace secondary windings by respective magnetizing inductance which are coupled and formed autotransformer. The negative terminal of the output stage represented by V_o , which was formerly connected to the central tap of the transformer, is then connected to the negative pole of the input voltage source to generate a boost topology.

Two modes of operations are described in 3SSC circuits in the basis of duty ratios. If duty ratio is larger than 0.5 overlapping mode is obtained, where two switches are conducted simultaneously. If duty ratio is less than 0.5 non overlapping mode is obtained, where two switches are operated in complementary. Only one switch is operated at an operating stage. The proposed circuit is an integration of interleaved technique and three state switching cell.

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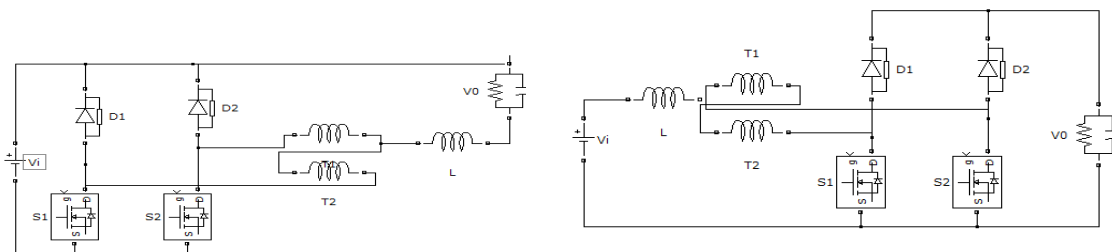
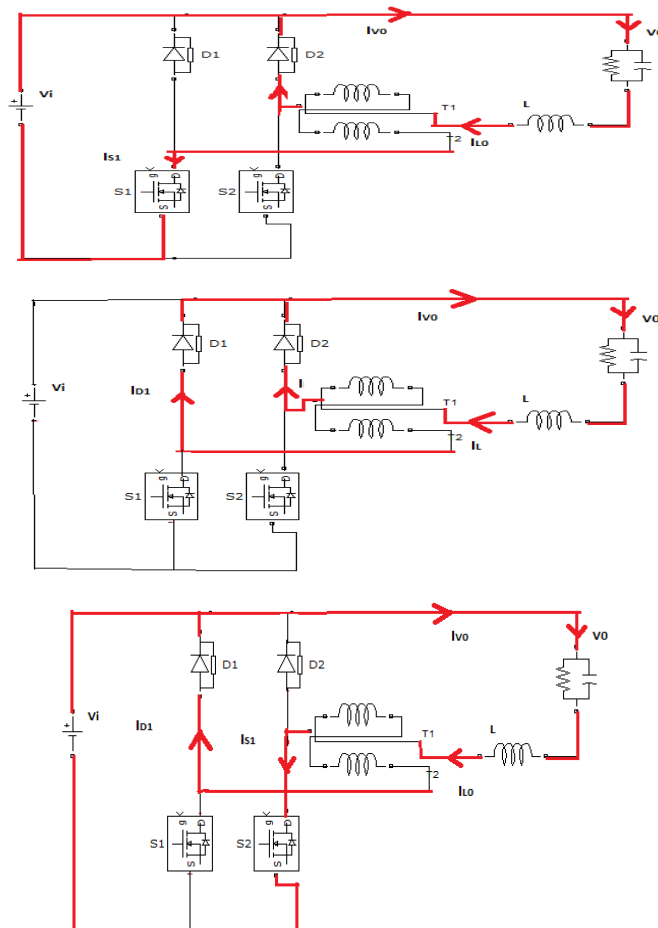


Fig. 1 Buck converter based on 3SSC Fig. 2 Boost converter based on 3SSC

A. Operating Stages Of Buck Converter Based 3SSC

Four modes of operations are performed in the buck converter based 3SSC.



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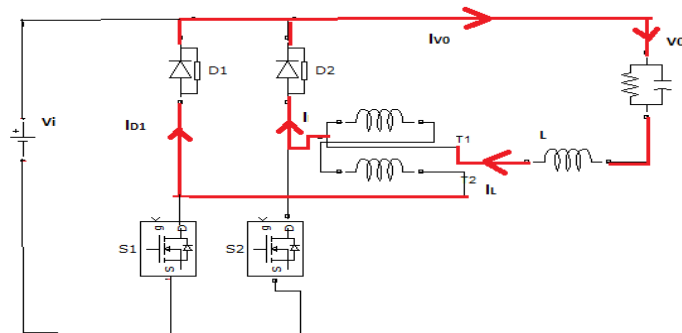


Fig 3. Operating stages of 3SSC buck converter

MODE 1: Initially, switch S_1 is turned ON, while switch S_2 is turned OFF. The current through the inductor is divided in two parts. The first one flows through T_2 and D_2 with energy being delivered to the load. The second one flows through T_2 and S_1 , current sharing is maintained since the number of turns for T_1 and T_2 is the same. The current through L increases linearly. Windings T_1 and T_2 have the same impedance, and the voltages across them are equal to half of the input voltage V_i . This stage finishes when S_1 is turned OFF [1].

MODE 2: Switch S_1 is turned OFF, while switch S_2 remains OFF. The voltage across inductor L is inverted. Diode D_1 is forward biased while D_2 remains conducting. The energy stored in L during the previous stage is then transferred to the load. The current flows through $T_1 T_2$, according to the given polarity, what causes the magnetic flow in the core to be null. The current returns to the source analogously to the previous stage. This stage finishes when S_2 is turned ON.

MODE 3: This stage is similar to the first one, although switch S_2 turned ON instead and S_1 remains turned OFF. Diode D_1 keeps conducting and D_2 is reverse biased.

MODE 4: This stage is similar to the second one, as the same equivalent circuit and operating conditions are valid in this case. [1]

IV. SIMULATION RESULTS

A. Simulink Model Of 3SSC Buck Converter

For simulating 3SSC buck converter, we use parameter values as $R=3.6$ ohm, $C=14.72 \times 10^{-6}$ F, $L=120 \times 10^{-6}$ H. Input voltage is taken as 200V. For pulse generation we use PWM generation and a controlled circuit is used to control output voltage. Output voltage is step downed and get 60V. Output current is 16 A. High output power 1KW is attained at duty ratio 0.3. As D varies output voltage also varies. D varies from 0.2 to 0.5.

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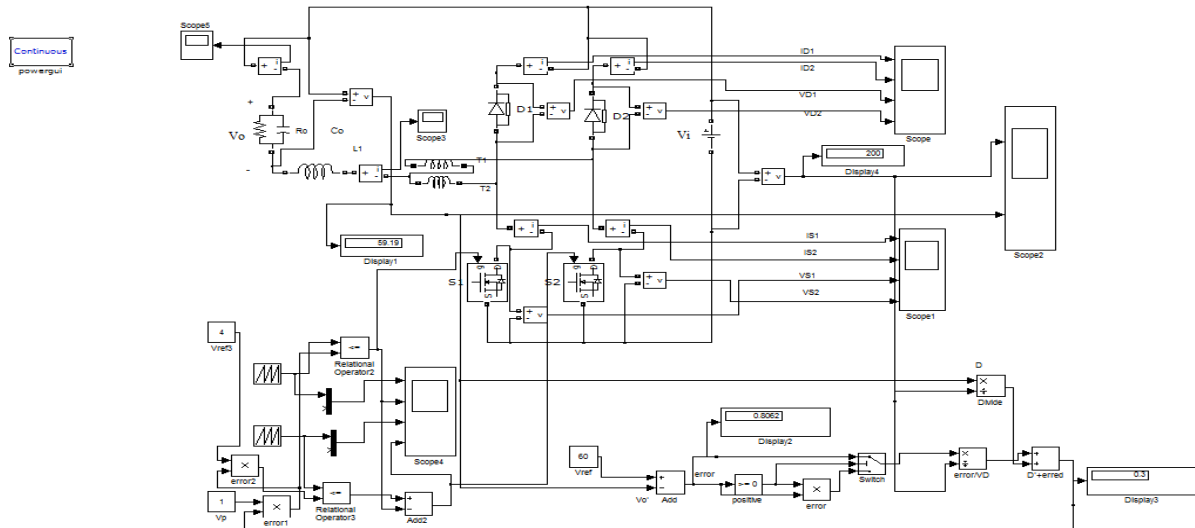


Fig 4. Simulink model of 3SSC buck converter

B. Simulink Model Of 3SSC Buck Converter

For simulating 3SSC boost converter, we uses parameter values as $R=3.6$ ohm, $C=14.72 \text{ e-}6$ F, $L=120\text{e-}6$ H. Input voltage is taken as 200V. For pulse generation we uses PWM generation and a controlled circuit is used to control output voltage. Output voltage is step upped and get 282V. Output current is 110 A.High output power 1.5KW is attained at duty ratio 0.3. As D varies output voltage also varies. D varies from 0.2 to 0.5.

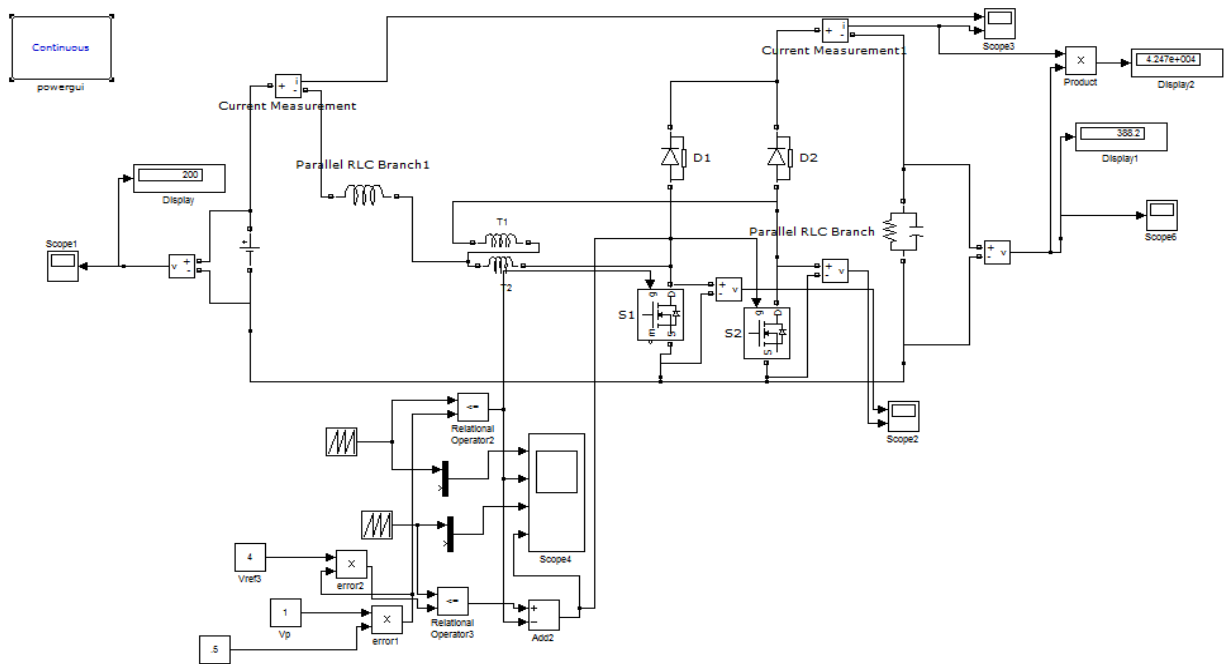


Fig 5. Simulink model of 3SSC boost converter

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Observing the simulation results, gate pulses given to two switches are complementary in action. Analysing the inductor current, the switching frequency is half of the ripple current frequency, it leads to the reduction of magnetic elements. 200V input of buck converter is stepped down to 60V and 200V of boost converter is stepped up as 282V at duty ratio 0.3.

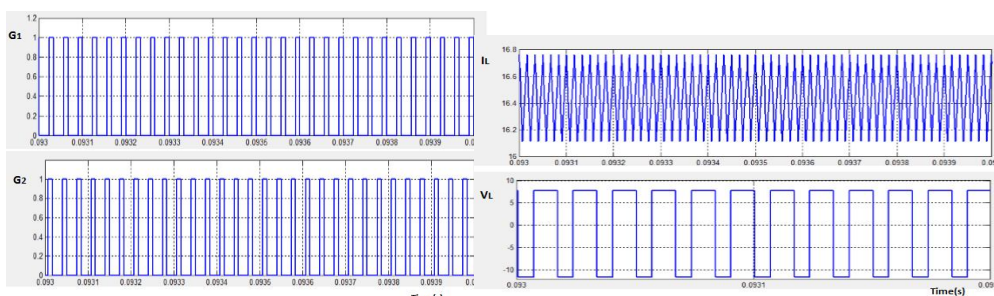


Fig. 6 Gate pulses for switches Fig. 7 Inductor current and voltage waveforms

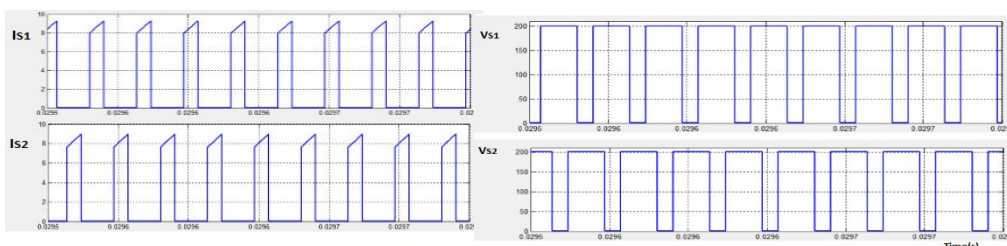


Fig. 8 switching current waveforms Fig. 9 switching voltage waveforms

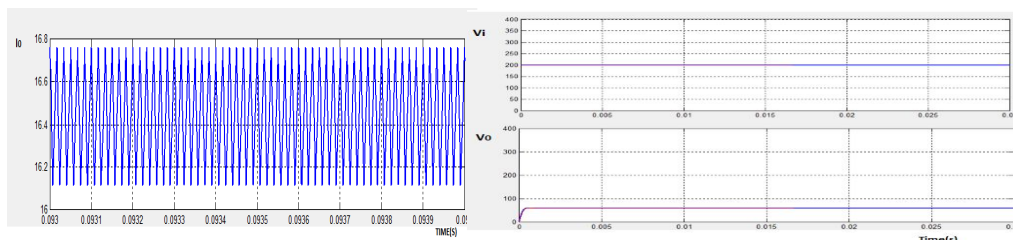


FIG. 10 OUTPUT CURRENT WAVEFORMS OF BUCK CONVERTER FIG. 11 INPUT AND OUTPUT VOLTAGE WAVEFORMS OF BUCK CONVERTER

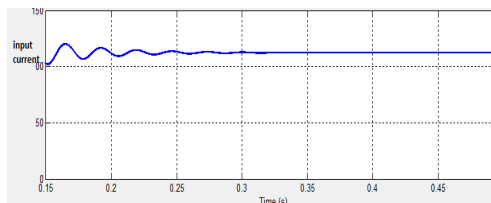


Fig. 12 Input current waveforms of boost converter

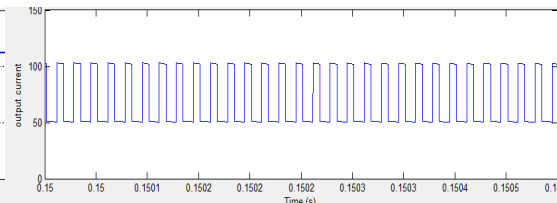


Fig. 13 Output current waveforms of boost converter

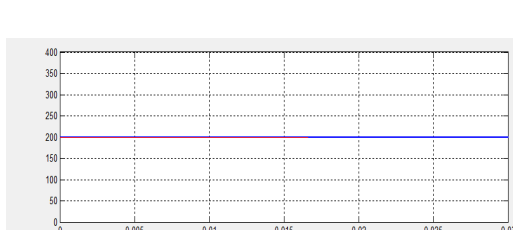


Fig. 14 Input voltage waveforms of boost converter

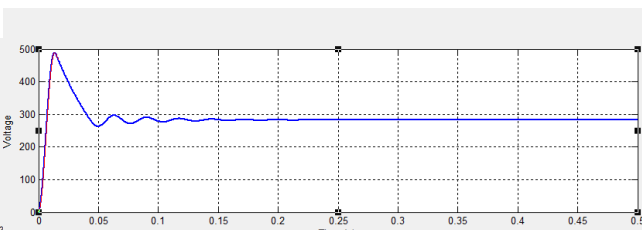


Fig. 15 Output voltage waveforms of boost converter



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TABLE I
DESIGN SPECIFICATIONS

PARAMETER	VALUE
Input Voltage	200 V
Inductor Current Ripple	3.33 A
Switching Frequency	30 kHz
Rated Output Power	1 kW
Output Voltage	60 V
Output Current	16.7 A
Output Voltage Ripple	0.6 V

TABLE II
VARIATION IN DUTY RATIOS

	DUTY RATIO	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT POWER
3SSC BUCK CONVERTER	0.2	200V	40V	432W
	0.3	200V	60V	1KW
	0.4	200V	80V	1.7KW
	0.5	200V	100V	2.7KW
3SSC BOOST CONVERTER	0.2	200V	246V	1.3KW
	0.3	200V	282	1.5KW
	0.4	200V	327	2.5KW
	0.5	200V	388	4.2KW

V.CONCLUSION

Step up and step down converter based on three state switching cell for high application were simulated and results are noted. In step down converter an input voltage 200 V is given and we got 60 V as output at duty ratio 0.3. Output will vary according to D from 0.2 to 0.5. A controlled feedback is given to the buck converter. Buck converter based on 3SSC gives 1 KW output power.

In Step up converter an input voltage 200 V is given and got 282 V as output and 110 A current, 1.5KW power at D equal to 0.3. Duty ratio will vary from 0.2 to 0.5. After 0.5 duty ratio overlapping mode will occur. Relationship between input-output voltages and duty ratio is observed as, in buck 3SSC converter $V_0/V_i = D$ and in boost 3SSC converter $V_0/V_i = 1/(1-D)$. Simulations are done in SIMULINK/MATLAB R2010a. From the simulation results high output power is obtained and less amount of ripples were observed.

REFERENCES

- Juan Paulo Robles Balastero, Fernando Lessa Tofoli, "A Dc-Dc Converter Based On The Three State Switching Cell For High Current And Voltage Stepdown Application," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 1394–1401, Jan. 2013
- J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, no. 8, pp. 728–734, Aug. 1997
- G. V. Torrico-Bascopé, R. P. Torrico-Bascopé, D. S. Oliveira, Jr., S. V. Araújo, F. L. M. Antunes, and C. G. C. Branco, "A high step-up converter based on three-state switching cell," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2006, pp. 998–1003
- R. P. Torrico-Bascopé, C. G. C. Branco, G. V. Torrico-Bascopé, C. M. T. Cruz, F. A. A. de Souza, and L. H. S. C. Barreto, "A new isolated DC–DC boost converter using three-state switching cell," in *Proc. Appl. Power Electron. Conf. Expo.*, 2008, pp. 607–613.
- J. P. R. Balestero, F. L. Tofoli, R. C. Fernandes, G. V. Torrico-Bascopé, and F. J. M. Seixas, "Power factor correction boost converter based on the three-state switching cell," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1565–1577, Mar. 2012.
- K. M. Smith, Jr. and K. M. Smedley, "Properties and synthesis of lossless, passive soft switching converters," in *Proc. 1st Int. Congr. Israel Energy Power Motion Control*, May 1997, pp. 112–119